REMARKS

An Excess Claim Fee Payment Letter is submitted herewith to cover the cost of two (2) excess dependent claim.

Claims 5-19 and 23-32 are all the claims presently pending in the application. Claims 20-22 have been canceled. Claims 5-7, 9-11, 17, 19 and 23-27 have been amended to further define the claimed invention. Claims 28-32 have been added to claim additional features of the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 5-7, 9-13, 15-16, 19-20 and 22-23 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Sunakawa, et al. Claims 9-13, 15 and 19-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sacuma, et al. Claims 17-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Yuri, et al. Claim 8 stands rejected under 35 U.S.C.§ 103(a) as being unpatentable over Sunakawa, et al. in view of Yamada, et al. (JP 7-169715). Claims 14 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sunakawa, et al. in view of Hino, et al. (U.S. Patent No. 6,682,991). Claims 24-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Davis, et al. (U.S. PG-Pub 2002/0148534).

These rejections are respectfully traversed in view of the following comments.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as recited in claim 5) is directed to a group III nitride compound semiconductor device including a silicon substrate on which a first environment division and a second environment division are formed, and a plurality of first group III nitride compound semiconductor layers formed on the first environment division so as to serve as effective semiconductor layers. Importantly, the first environment division includes a surface of the silicon substrate, the plurality of first group III nitride compound semiconductor layers being

formed on the surface, and the second environment division includes silicon oxide formed on the surface of the silicon substrate.

Another exemplary aspect (e.g., as recited in claim 9) is directed to semiconductor device structure having a first portion and a plurality of second portions. The structure includes a silicon substrate, a silicon oxide separating layer formed on the surface of the substrate and defining a plurality of openings respectively formed in the plurality of second portions, and a plurality of stacks of group III nitride compound layers which are respectively formed on the surface in the plurality of openings.

Another exemplary aspect (e.g., as recited in claim 17) is directed to a method of forming a semiconductor device structure having a first portion and a plurality of second portions. The method includes forming a silicon oxide separating layer over a surface of a silicon substrate, forming a mask over the separating layer, etching the separating layer using the mask to create a plurality of openings in the separating layer, and forming a plurality of group III nitride compound semiconductor layers on the surface of the silicon substrate in the plurality of openings.

Another exemplary aspect (e.g., as recited in claim 24) is directed to a method of forming a group III nitride compound semiconductor device. The method includes forming amorphous silicon portions of a silicon substrate surface in a grid-shaped pattern by implanting ions in the silicon substrate surface, and forming a group III nitride compound semiconductor layer on the substrate surface such that a portion of the layer formed on the amorphous silicon portions of the substrate surface has a different crystalline structure than a portion of the layer formed on portions of the substrate surface that are other than the amorphous silicon portions.

In conventional methods, a stress due to a thermal expansion coefficient difference between the group III nitride compound semiconductor layer and the substrate causes cracks in the group III nitride semiconductor layer (Application at page 1, lines 13-23).

The claimed invention, on the other hand, may form (e.g., individually and separately form) the group III nitride layers in areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking

(Application at page 2, line 17-page 3, line 4).

II. THE PRIOR ART REFERENCES

A. The Sunakawa Reference

The Examiner alleges that Sunakawa teaches the claimed invention of claims 5-7, 9-13, 15-16, 19-20 and 22-23. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Sunakawa.

Specifically, Applicant submits that Sunakawa does not teach or suggest "*wherein said first environment division comprises a surface of said silicon substrate, said plurality of first group III nitride compound semiconductor layers being formed on said surface, and wherein said second environment division comprises silicon oxide formed on said surface of said silicon substrate*", as recited in claim 5, nor "*a plurality of stacks of group III nitride compound layers which are respectively formed on said surface in said plurality of openings*", as recited in claim 9.

As noted above, unlike conventional devices, the claimed invention may form (e.g., individually and separately form) the group III nitride layers in areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking (Application at page 2, line 17-page 3, line 4).

Clearly, these features are not taught or suggested by Sunakawa. Indeed, Applicant would point out to the Examiner that in the claimed invention, the substrate includes silicon, the first environment division may correspond to the surface of the silicon substrate, the second environment division includes silicon oxide, and a mask layer may be formed on the group III nitride compound semiconductor device.

Specifically, in a first exemplary embodiment of the claimed invention, the second environment division (including silicon oxide) is formed on the silicon substrate. According to the exemplary aspects of the claimed invention, the group III nitride semiconductor device (e.g., GaN) is not necessarily formed on the silicon oxide. GaN may be formed only in the first environment division, which corresponds to the silicon substrate.

By such composition, the GaN may be grown in small areas on the substrate individually and separately so that the areas are not connected to one another (e.g., see the attached Exhibit 1 which is incorporated by reference herein). Thus, the invention enables a reduction of the stress accumulated inside of the semiconductor layers.

The Examiner attempts to rely on Figures 4-5 in Sunakawa to support his position. However, these Figures teach a GaN layer 42 formed over the entire surface of the substrate 41, and a mask 33 formed on the GaN layer 42. Nowhere do these figures teach or suggest a first environment division including a surface of the silicon substrate, the plurality of first group III nitride compound semiconductor layers being formed on the surface, and the second environment division including silicon oxide formed on the surface of the silicon substrate. Nor do the figures teach or suggest a plurality of stacks of group III nitride compound layers which are respectively formed on the surface in said plurality of openings.

On the contrary, in Sunakawa the mask is formed on the surface of the GaN layer 42, not on the surface of a silicon substrate. Likewise, the facet structures 46 are formed on the surface of the GaN layer 42, not on the surface of a silicon substrate. Thus, the Sunakawa device is clearly unrelated to the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Sunakawa. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Sakuma Reference

The Examiner alleges that Sakuma teaches the claimed invention of claims 9-13, 15, 19 and 20. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Sakuma.

Specifically, Applicant submits that Sakuma does not teach or suggest "*a plurality of stacks of group III nitride compound layers which are respectively formed on said surface in said plurality of openings*", as recited in claim 9. As noted above, this allows the claimed invention to form (e.g., individually and separately form) the group III nitride layers in areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III

nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking (Application at page 2, line 17-page 3, line 4).

Clearly, these features are not taught or suggested by Sakuama. Indeed, the Examiner attempts to rely on figures 1 and 23 in Sakuma to support his position. However, the Examiner is clearly incorrect.

Indeed, Figure 1 merely teaches a silicon dioxide layer 2 formed on a compound semiconductor layer (that is, not formed on a silicon substrate), and a hole 3 formed in the silicon dioxide layer 2. Figure 23 merely teaches a silicon dioxide layer 152 formed on a GaAs substrate 151 (that is, not formed no a silicon substrate).

In short, nowhere does Sakuma teach or suggest a plurality of stacks of group III nitride compound layers which are respectively formed on the surface of the silicon substrate in the plurality of openings. Thus, Sakuma is completely unrelated to the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Sakuma. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Yuri Reference

The Examiner alleges that Yuri teaches the claimed invention of claims 17 and 18. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Yuri.

Specifically, Applicant submits that Yuri does not teach or suggest "*forming a plurality of group III nitride compound semiconductor layers on said surface of said silicon substrate in said plurality of openings* ", as recited in claim 17. As noted above, this allows the claimed invention to form (e.g., individually and separately form) the group III nitride layers in areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking (Application at page 2, line 17-page 3, line 4).

Clearly, these features are not taught or suggested by Yuri. Indeed, the Examiner attempts to rely on Figures 7, 15 and 23 in Yuri to support his position. However, the Examiner

is clearly incorrect.

Indeed, Figures 7, 15 and 23 merely teach a silicon dioxide layer 2 formed on a silicon substrate 7, and a silicon layer 8 formed on the silicon dioxide layer 2. Openings are formed in the layers 2 and 8 and a silicon carbide layer 9 formed on the silicon layer 8 and in the openings. A GaN layer 4 is then formed on the silicon carbide layer 9, not in the openings and not on the surface of the silicon substrate 7.

In short, nowhere does Yuri teach or suggest forming a plurality of group III nitride compound semiconductor layers on the surface of the silicon substrate in said plurality of openings. Thus, Yuri is completely unrelated to the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Yuri. Therefore, the Examiner is respectfully requested to withdraw this rejection.

D. The Yamada and Hino References

The Examiner alleges that Sunakawa would have been combined with Yamada to form the invention of claim 8, and with Hino to form the invention of claims 14 and 21. Applicant submits, however that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention.

Applicant respectfully submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination.

Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant submits that neither Sunakawa, nor Yamada, nor Hino, nor any

alleged combination of these references, teach or suggest "*wherein said first environment division comprises a surface of said silicon substrate, said plurality of first group III nitride compound semiconductor layers being formed on said surface, and wherein said second environment division comprises silicon oxide formed on said surface of said silicon substrate*", as recited in claim 5, nor "*a plurality of stacks of group III nitride compound layers which are respectively formed on said surface in said plurality of openings*", as recited in claim 9.

Clearly, these features are not taught or suggested by Sunakawa. Indeed, with respect to Yamada, the substrate is composed of sapphire, and the grooves are formed thereon. Then, Yamada forms the GaN on the whole surface of the substrate, and then removes the GaN with bad crystallinity grown on the grooves. Thus, the device and production method of the present invention is completely different from the Yamada method.

Moreover, the claimed device is clearly distinguished from Yamada, since the composition of the substrate is different. Therefore, Yamada clearly fails to make up for the deficiencies in Sunakawa.

Likewise, Hino does not teach or suggest the novel features of the claimed invention. Indeed, the Examiner attempts to rely on Figure 11 in Hino to support his position. However, Figure 11 merely teaches a GaN layer 2 formed on a sapphire substrate 1, and a growth mask 7 formed on the GaN layer 2.

Thus, like Yamada, nowhere does Hino teach or suggest a first environment division including a surface of the silicon substrate, the plurality of first group III nitride compound semiconductor layers being formed on the surface, and the second environment division including silicon oxide formed on the surface of the silicon substrate, or a plurality of stacks of group III nitride compound layers which are respectively formed on the surface in said plurality of openings.

Therefore, Applicant submits that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

E. The Davis Reference

The Examiner alleges that Davis would have been combined with Yuri to form the invention of claims 24-27. Applicant submits, however that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention.

Applicant respectfully submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

In fact, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination.

Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant submits that neither Davis, nor Yuri, nor any combination thereof, teaches or suggests "*forming a group III nitride compound semiconductor layer on said substrate surface such that a portion of said layer formed on said amorphous silicon portions of said substrate surface has a different crystalline structure than a portion of said layer formed on portions of said substrate surface that are other than said amorphous silicon portions*", as recited in claim 24. As noted above, the claimed may form (e.g., individually and separately form) the group III nitride layers in areas which are not connected to one another. Thus, even when the thermal expansion coefficient of the group III nitride layer is different than the coefficient for the substrate, stress accumulated in the layer is small, thereby inhibiting cracking (Application at page 2, line 17-page 3, line 4).

Clearly, these features are clearly not taught or suggested by Davis. Indeed, the Examiner attempts to rely on Figures 1-8 in Davis to support his position. However, the Examiner is clearly incorrect.

Indeed, Figures 1-8 in Davis merely teach a sapphire or GaN substrate 102a, an AlN layer

102b formed on the substrate 102a, a GaN layer 104 formed on the AlN layer 102b, and a silicon dioxide mask 106 formed on the GaN layer 104. A first lateral GaN layer 108b is then formed on the silicon dioxide mask 106. Thus, Davis is completely unrelated to the claimed invention in which a group III nitride compound semiconductor layer is formed on a silicon substrate surface such that a portion of the layer formed on amorphous silicon portions of the silicon substrate surface has a different crystalline structure than a portion of the layer formed on portions of the silicon substrate surface that are other than the amorphous silicon portions.

Likewise, these novel features are not taught or suggested by Yuri. Indeed, the Examiner again attempts to rely on Figures 7, 15 and 23 to support his position. However, these Figures merely teach a GaN layer 4 formed on a silicon carbide layer 9, not on the surface of the silicon substrate 7. Thus, Yuri is completely unrelated to the claimed invention.

Therefore, Applicant submits that these references would not have been combined and even if combined, the alleged combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

Applicant notes that the Notice of References Cited which was included in the Office Action dated July 13, 2004 included some errors. Namely, the inventor of JP2000-77336A should be "Hara", with regards to JP10-233385A, the inventor should be "Yuasa et al" and the publication date should be September 2, 1998, and JP2000-331940 (inventor "Anzai", published on November 30, 2000) should be added to the list (see the Attached Exhibits 2-4 which include the PAJs for the aforementioned documents).

In view of the foregoing, Applicant submits that claims 5-19 and 23-32, all the claims pending and presently being examined in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Applicant submits that regarding the Notice of References Cited, there are errors in the list of Foreign Patent Documents. First, the inventor of JP2000-77336A is "Hara". Second,

regarding JP10-233385A, the inventor should be amended as "Yuasa et al." and the publication date should be amended as "September 2, 1998". Third, JP2000-331940A (inventor "Anzai", published on November 30, 2000) should be added into the list. (See attached PAJs).

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 10/13/04

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Ahmed N. Sefer, Group Art Unit # 2826 at fax number (703) 872-9306 this 13th day of October, 2004.

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